

WHAT IS CLAIMED IS:

1. A magnetic memory comprising:
an insulator having a trench;
a first conductor in the trench;
a first magnetic layer in the trench and adjacent to the first conductor;
and
a second magnetic layer outside the trench.
2. The magnetic memory of claim 1, comprising a barrier layer outside the trench and disposed between the first magnetic layer and the second magnetic layer.
3. The magnetic memory of claim 1, comprising a barrier layer that prevents shorts between the first magnetic layer and the second magnetic layer.
4. The magnetic memory of claim 1, where the first magnetic layer is self-aligned with the first conductor along at least one dimension of the trench.
5. The magnetic memory of claim 1, where the first magnetic layer comprises a reference layer.
6. The magnetic memory of claim 1, where the second magnetic layer is patterned into bits aligned with the first magnetic layer.
7. The magnetic memory of claim 1, comprising a second conductor disposed over the second magnetic layer, where the second conductor is narrower than the second magnetic layer.
8. The magnetic memory of claim 1, comprising a second conductor disposed over the second magnetic layer, where the second conductor is

patterned into lines and the first magnetic layer is patterned into bits with a line mask pattern.

9. The magnetic memory of claim 1, comprising a second conductor disposed over the second magnetic layer and a barrier layer disposed between the first magnetic layer and the second magnetic layer, where the second conductor and the second magnetic layer are patterned the same.

10. The magnetic memory of claim 1, where the first magnetic layer comprises a sense layer.

11. The magnetic memory of claim 1, where the first conductor comprises:
a ferromagnetic cladding layer lining the trench; and
copper.

12. A magnetic memory comprising:
an array of memory cells;
first conductive lines;
second conductive lines crossing the first conductive lines at memory cells in the array of memory cells, where a memory cell in the array of memory cells comprises:

a first magnetic layer inside an insulating recess;
a second magnetic layer outside the insulating recess; and
a barrier layer between the first magnetic layer and the second magnetic layer.

13. The magnetic memory of claim 12, where the barrier layer is in a plane over the insulating recess.

14. The magnetic memory of claim 12, where the first conductive lines are in parallel insulating trenches formed in an insulator.

15. The magnetic memory of claim 12, where the array of memory cells is a three dimensional macro-array.
16. The magnetic memory of claim 12, comprising a write circuit configured to provide write currents to set memory cell states and a read circuit configured to provide a sense voltage and a sense current to read memory cell states.
17. The magnetic memory of claim 12, where the first magnetic layer crosses a plurality of memory cells.
18. A magnetic memory comprising:
 - means for self-aligning at least one dimension of a magnetic layer with a conductor in a dielectric; and
 - means for supporting a planar barrier layer adjacent to the magnetic layer and the dielectric layer.
19. The magnetic memory of claim 18, where the means for self-aligning comprises side surfaces of a trench in the dielectric.
20. The magnetic memory of claim 18, where the means for supporting a planar barrier layer comprises the magnetic layer and the dielectric planarized to a planar surface.
21. A magnetic memory cell comprising:
 - a first magnetic layer in a recess in a dielectric;
 - a barrier layer formed in a plane on the first magnetic layer and the dielectric; and
 - a second magnetic layer formed on the barrier layer.
22. The magnetic memory cell of claim 21, where the first magnetic layer is a sense layer and the second magnetic layer is a reference layer.

23. The magnetic memory cell of claim 21, where the first magnetic layer is a reference layer and the second magnetic layer is a sense layer.
24. A method of forming a magnetic memory comprising:
forming a recess in a dielectric;
coating the dielectric with a first magnetic layer;
removing the first magnetic layer from outside the recess; and
forming a second magnetic layer outside the recess.
25. The method of claim 24, where forming the recess comprises:
forming a trench in the dielectric;
depositing conductive material in the trench; and
removing conductive material to form the recess in the trench.
26. The method of claim 25, where depositing conductive material comprises:
depositing ferromagnetic cladding to line the trench; and
depositing copper to fill the lined trench.
27. The method of claim 25, where removing conductive material comprises at least one from a group comprising etching the conductive material with an ion etch, etching the conductive material with a wet chemical etch and polishing the conductive material with a chemical mechanical polish.
28. The method of claim 24, where coating the dielectric comprises depositing a blanket first magnetic layer.
29. The method of claim 24, where coating the dielectric comprises depositing a blanket first magnetic layer and a blanket sacrificial layer.
30. The method of claim 24, where removing the first magnetic layer comprises polishing with a chemical mechanical polish to form a planar surface.

31. The method of claim 24, comprising:
forming a barrier layer between the first magnetic layer and the second magnetic layer; and
forming a second conductor over the second magnetic layer.
32. The method of claim 31, where forming the barrier layer comprises forming a blanket barrier layer over the dielectric and the first magnetic layer.
33. The method of claim 31, where forming the second magnetic layer comprises using a bit mask and forming the second conductor comprises using a line mask.
34. The method of claim 31, where the first magnetic layer, the barrier layer, the second magnetic layer and the second conductor are patterned using a line mask.